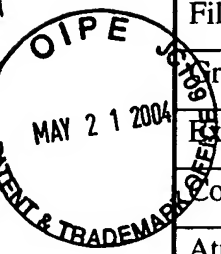


First Named Inventor	Leonard Forbes	GENERAL TRANSMITTAL FORM UNDER 37 CFR 1.8 (LARGE ENTITY)
Serial No.	10/612,725	
Filing Date	July 1, 2003	
Group Art Unit	2811	
Examiner Name	Unknown	
Confirmation No.	5767	
Attorney Docket No.	400.258US01	
Title: APPARATUS AND METHOD FOR SPLIT TRANSISTOR MEMORY HAVING IMPROVED ENDURANCE		

Mail Stop Amendment
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Enclosures					
The following documents are enclosed:					
<input checked="" type="checkbox"/>	Supplemental Information Disclosure Statement (1 pg.); Form 1449 (7 pgs.); 58 copies of cited references; U.S. reference(s) not included pursuant to 37 C.F.R. 1.98 (c)(2)(i);				
<input checked="" type="checkbox"/>	An itemized return-receipt postcard				
Leffert Jay & Polglaze, P.A. P.O. Box 581009 Minneapolis, MN 55458-1009 T - 612/312-2200 F - 612/312-2250					
Please charge any additional fees or credit any overpayments to Deposit Account No. 501373.					
CUSTOMER NO. 27073					
Submitted By					
Name	Andrew C. Walseth	Reg. No.	43,234	Telephone	(612) 312-2207
Signature				Date	5/19/04
Certificate of Mailing					
I certify that this correspondence and the identified documents listed on this transmittal are being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450 on May 19, 2004.					
Name	Rhonda L. Foley		Signature		

(LARGE ENTITY TRANSMITTAL UNDER 37 CFR § 1.8)



First Named Inventor	Leonard Forbes	SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT
Serial No.	10/612,725	
Filing Date	July 1, 2003	
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In compliance with 37 C.F.R. §§ 1.56 and 1.97, *et seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified Application. Pursuant to 37 C.F.R. 1.98 (a)(2)(ik), as this application was filed after June 30, 2003, Applicant has not included copies of U.S. Patents or U.S. Patent Applications. Applicant respectfully requests that this Supplemental Information Disclosure Statement be entered and the references listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to MPEP §609, Applicant further requests that the Examiner initial next to each reference on the Form 1449 to indicate that the listed references have been considered. Applicant further requests that a copy of the initialed Form 1449 be returned with the next official communication.

As an Office Action has not yet issued in this application, Applicant believes that no fees are due. However, the Commissioner for Patents is hereby authorized to charge any additional fees to Deposit Account No. 501373. If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2207.

Respectfully submitted,

Date: 5/19/04



Andrew C. Walseth
Reg. No. 43,234

Attorneys for Applicant
Leffert Jay & Polglaze
P.O. Box 581009
Minneapolis, MN 55458-1009

T 612 312-2200
F 612 312-2250



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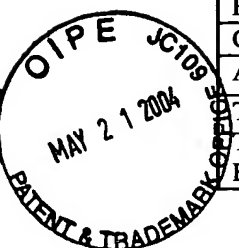
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